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NATURAL CONVECTIVE AIR COOLING OF THE PCBs ARRAY IN A CLOSED CASING

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Abstract

An experimental investigation was carried out to study the natural convective air cooling of the printed-circuit-boards (PCBs) array which was set up vertically in a closed casing. The results show that there exists an unstable thermal boundary layer on the top wall, which brings about vortex flow and temperature oscillation in the casing. Because of the thermal instability the air circulation in the casing is unsteady. Time-varying recirculation presents in the PCBs array. Experimental results were correlated in the form of $Nu = f(Ra, r)$ with Rayleigh-number ranging from 10^2 to 10^5 at $Pr = 0.71$.

1 INTRODUCTION

Natural convection cooling technique has been widely used in electronic industry. Especially in the electronic equipments with low power and packaging density natural convection cooling methods are often preferred to maintain the temperature below an acceptable level. In some adverse circumstances where the casing of the electronic equipment must be closed for dust- and water-proof, natural convection cooling scheme may be the only feasible option. Therefore, it is necessary to investigate in detail the natural convection process in such complex structure in order to achieve the optimum cooling effect. Electronic equipments, which consist of several printed-circuit-boards (PCBs) that are grouped into an array and set up in a closed casing, were considered in this paper.

In the pioneering paper by Elenbaas [1942] the thermal characteristics between two isothermal parallel plates were first reported. It was showed that the Nusselt number based on the spacing between the plates is proportional to $b/h \cdot Gr \cdot Pr = b/h \cdot Ra$. The optimum spacing was also analyzed in his paper. Much work has been done on the natural convection between two parallel plates under various boundary conditions (summerized by Johnson [1986]), which set up the foundation of studying natural convection cooling in electronic equipments. Some factors that have influence on the natural convection and heat transfer in electronic equipments, such as PCBs spacing, additional plates, the shape and size of the vents etc., were studied by Guglielmini [1985, 1988a, 1988b]. Cadre [1988] and Liu [1988] reported the numerical simulations of natural convection cooling of the PCBs array in a casing.

The present work is concerned with experimental investigation of natural convective air cooling of the PCBs array in a closed casing. The heat transfer and air flow in such PCBs array have been measured with holographic interferometer and LDV. From experimental results empirical correlations were deduced. The effects of the spacing between PCBs, distance between the PCBs array and top or bottom wall of the casing and the instability were analyzed.

2 EXPERIMENTS

2.1 Test Section

Edge and side view of the test section are shown in Fig.1. The simulated PCBs were 220.0 mm long by 120.0 mm high and 10.0 mm thick, constructed of the copper foil laminates similar to that used in electronic industry. Heater elements were designed as a serpentine fashion formed on the laminates with etch method. Two laminates were mounted on two sides of a frame to make one simulated PCB. Voltage

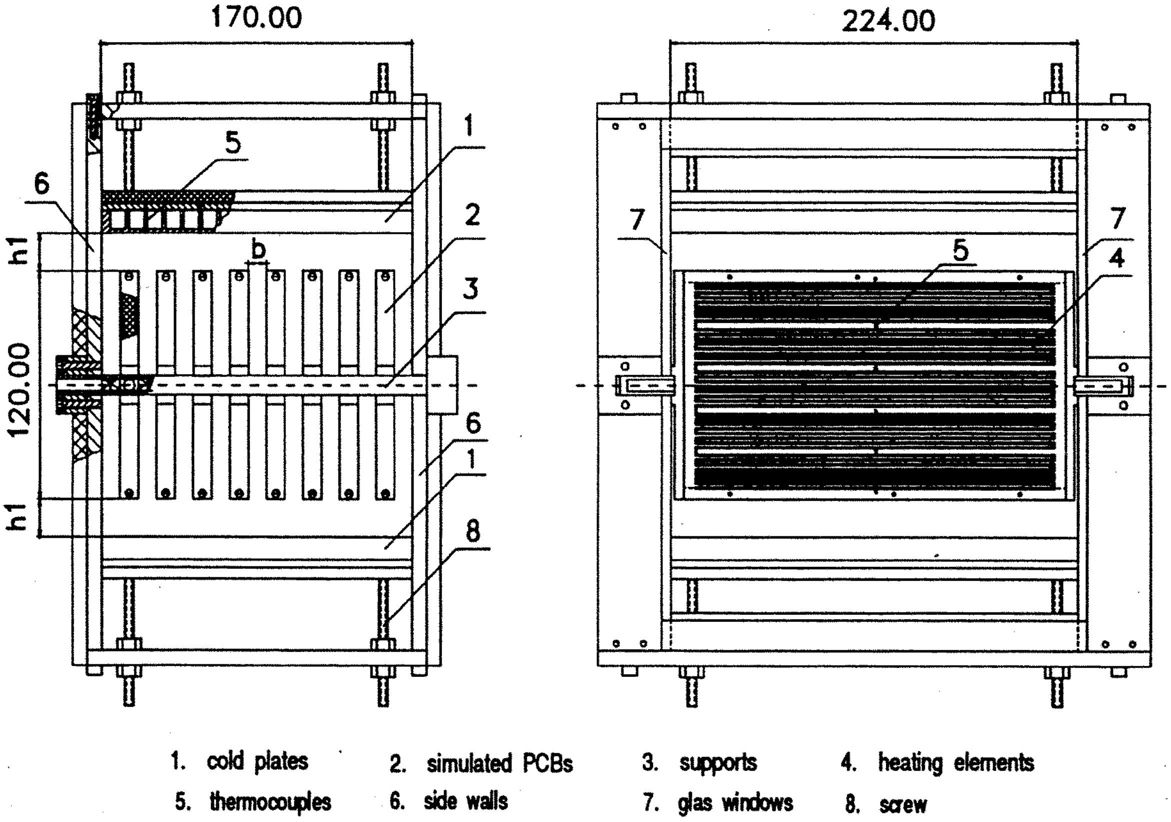


Figure 1: Test section

and current measurements were made for each heater element giving an estimated accuracy ±3%.

The top and bottom wall of the casing were made of aluminium plates. S-form slots were cut in the plates. Cold water from a thermostat was used to cool the top and bottom wall at constant temperature $20°C$. The side walls were made of plexiglass plates ($k \approx 0.184 W/°Km$). The front and the back wall were glass windows for the holographic interferometer and LDV. The spacings among PCBs were equal and could be changed. The distances between the PCBs array and the top or bottom wall were also adjustable through a screw mechanism.

2.2 Measuring Technique

Temperature field in the PCBs array was measured by a ϕ 150mm holographic interferometer. In order to trace the unstable thermal boundary layer occurring in the casing, real time holographic interferometry was used to visualize the temperature field. The principle of real time holographic interferometry was discussed in detail by F. Mayinger [1974].

The local Nusselt number can be expressed as follows:

$$Nu_x = \frac{b\dot{q}}{k(T_p - T_w)} = f(Ra, r) \qquad (1)$$

where Nu_x is the local Nusselt number, b the PCBs spacing, T_p the temperature on the PCB, T_w the temperature of the top wall, Ra the modified channel Rayleigh number and r the geometric parameter. Ra is defined as:

$$Ra = \frac{g\beta\dot{q}b^5}{k\alpha\nu H} \qquad (2)$$

where H is the height of the PCB.

The wall temperature was measured by 0.2 mm chromel/alumel thermocouples. Six thermocouples were spaced at the same interval along each side of the PCB and located in the 2-mm wide gaps between the heater strips. The velocity profile in the channel between two PCBs was measured by a Laser-Doppler-Velocimeter (LDV). Standard technique was applied.

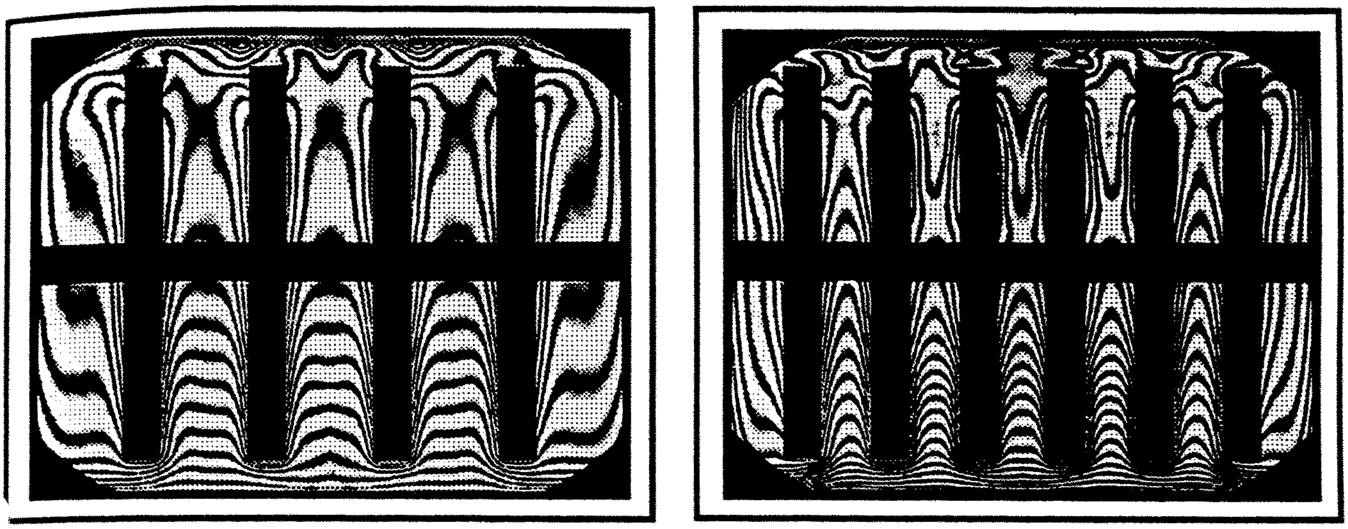


Figure 2: Holographic interferograms in 4- and 6-PCBs arrays

3 RESULTS

3.1 Temperature Fields

The holographic interferograms of temperature fields in 4- and 6-PCBs arrays are, for instance, shown in Fig.2 (For the sake of clarity the right halves of the above holograms are presented with the mirror images of the left halves.).

From Fig.2 it can be observed that the thermal boundary layers present on the surfaces of PCBs because of the natural convection. When the PCBs spacing is relatively large (e.g. in 4-PCBs array), thermal boundary layers are in evidence along each surface. In the lower half part of PCBs channels, the thermal boundary layers develop from bottom to top and become thicker as expected. However in the exit region of the channels, the development of the thermal boundary layer is hindered by the vortex flow which is produced by the thermal instability in the reverse temperature layer on the top wall of the casing. The thickness of the thermal boundary layer is reduced by cold air which falls randomly down from top wall. The thermal boundary layers in the PCBs array have therefore a bulging form. When the PCBs spacing is small enough (e.g. in 6-PCBs array) the developing boundary layers in the channels join together behind a short developing region. It is obvious that the ability of heat removal for small PCBs spacing in single channel is lower than that for large PCBs spacing. However, for the former the power load on each PCB which needs to be removed will be reduced because of more PCBs available in the casing. Therefore, one optimum spacing may be found for the optimum cooling effect, which will be discussed later.

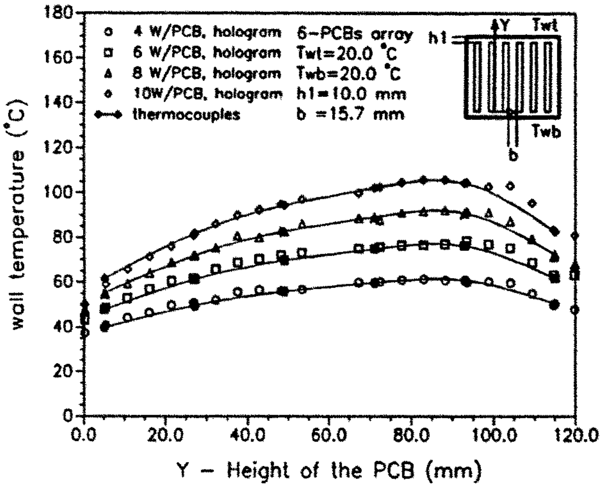
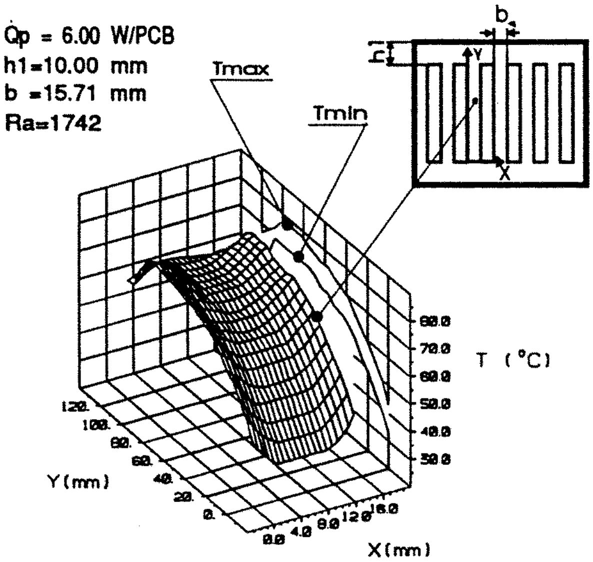


Figure 3: Temperature on the PCB

The temperature distributions on the PCB in a 6-PCBs array are shown in Fig.3. The maximum of the surface temperature presents at about 3/4 height of the PCB. The temperature profile in the related channel is presented in Fig.4.



Temperature profile in one of the channels of 6-PCBs array

Figure 4: Temp. profile in the channel

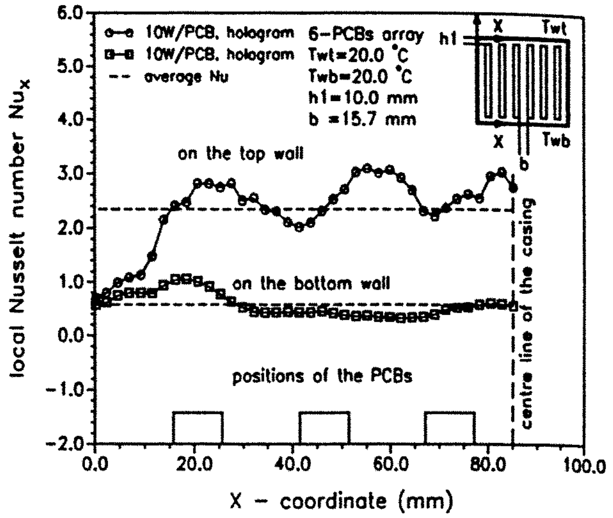


Figure 5: Nu on the top and bottom wall

On the top wall of the casing the thermal boundary layer has a wavelike form. The cold air on the top wall sinks down from the wave crest into the PCBs array and interacts with the warm air rising up from the channels to produce vortex flow in the exit region of the PCBs array. Because of this time-varying falling of cold air temperature in this region is unsteady. With increasing Rayleigh number the temperature oscillation changes from periodic to chaotic. These temperature oscillations attenuate from the centre of the channels to the surfaces of the PCBs. On the surface of the PCBs the temperature oscillates only in the limit of 0.4°C.

3.2 Heat Transfer

By means of an image processing system, the interference fringe can be measured quantitatively. The heat transfer coeffiecient can be calculated with equations in previous section. As an example, the local Nusselt numbers at the various points on the top wall and the bottom wall are shown in Fig.5. The fluctuation of heat transfer coefficient resulted from the thermal instability can be clearly seen from Fig.5. It can be also found from Fig.5 that the waveform of the $Nu_x - X$ curve corresponds to the corrugated form of the thermal boundary layer on the top wall of the casing. The wave trough of the $Nu_x - X$ curve is in accordance with the wave crest of the thermal boundary layer, where the air in vortex flow leaves the top wall. The wave crest of the $Nu_x - X$ curve is in accordance with the wave trough of the thermal boundary layer, where the air in vortex flow goes to the top wall. The average Nusselt number on the top wall is 3 $\sim$ 5 times higher than that on the bottom wall.

For the thermal design of electronic equipments the relation between total heat load and temperature difference is very important. Determining the total heat load according to the given permitted temperature rise and/or finding the maximum temperature rise on the basis of the given total heat load is one of fundamental tasks of thermal designers. From the experimental results correlation between Nusselt number and Rayleigh number can be expressed as follows:

$$Nu_p = 0.1163 Ra^{0.287} \tag{3}$$

where Nu_p is defined as:

$$Nu_p = \frac{b\dot{q}}{k(T_{p_{max}} - T_w)} \tag{4}$$

where $T_{p_{max}}$ is maximal temperature in the PCBs array. This correlation is shown in Fig.6.

When the distance between the PCBs array and top wall is increased, the flow resistance in the PCBs array will be reduced. Because of the limitation of the side channel the air circulation can only be accelerated to a certain degree. In addition, the direct

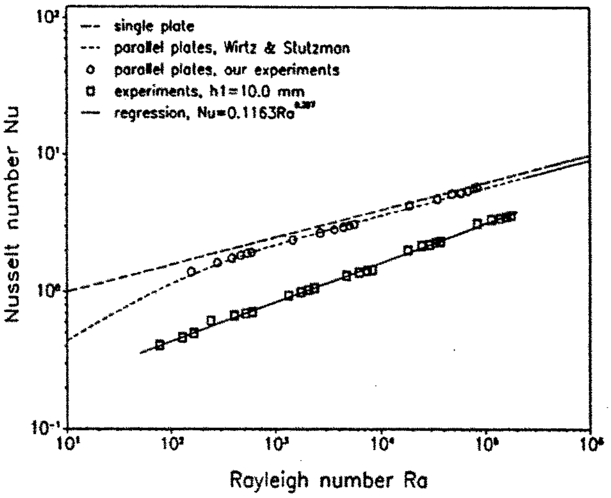


Figure 6: Relation $Nu_p = f(Ra)$

cooling effect of the top wall on the PCBs array will be also on the decrease as the distance between the PCBs array and the top wall increases. Because of these two opposite factors the cooling effect of the PCBs array will be insensitive to the distance between the PCBs array and top wall, which has been confirmed by experiments.

3.3 Velocity Profile in PCBs Array

Air circulation plays an important role in the cooling of the PCBs array in a closed casing. The air goes up from the PCBs array when it is warmed up by the dissipation heat of chips on the PCBs. Because of the existence of the top wall air flow has to take a turn to two side walls of the casing. When the side walls of the casing are cold the air flow falls down in the two side channels and rises again into the PCBs array after a turn on the bottom wall. As a whole, the overall natural convection flow can be divided into several circulation layers. When the situation is symmetrical the natural convective air flow produced in the central channel circulates in the most external layer and air stream from the channels next to the central one flows around the interior layers in sequence.

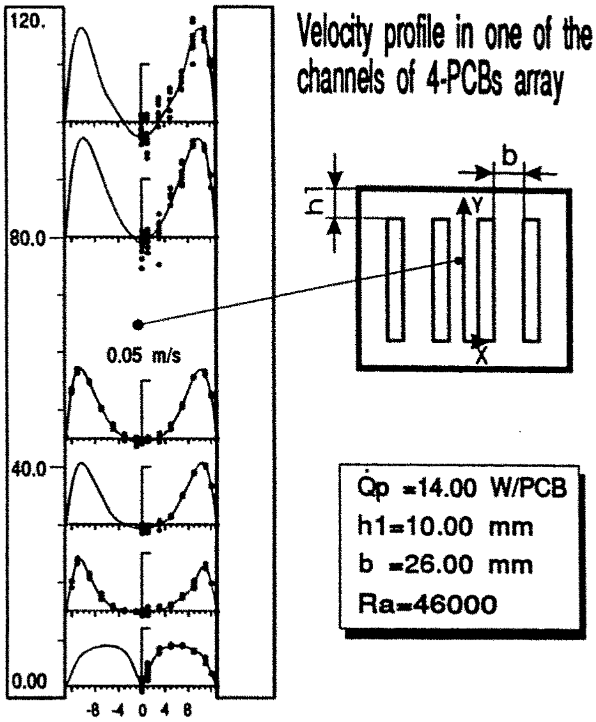


Figure 7: Velocity profile

In order to confirm the existence of the recirculation in the PCBs array the velocity profile in the central channel between two PCBs was measured with LDV. Fig.7 presents these measuring results. From Fig.7 it can be seen that the recirculation exists in the central part of the channel. The penetration of the recirculation is till the half height of PCBs. In the exit region the velocity is also unsteady because of the time-varying recirculation. It can be clearly seen that the thickness of the boundary layer is the largest at the entrance because of the 90° turn of the air flow from the side channels. It increases in the channel as expected and decreases at the exit region because of the recirculation.

3.4 Optimum PCBs spacing

As mentioned above there may exist an optimum arrangement of PCBs under the same maximal temperature difference between the PCBs array and the cold wall due to the ability of heat removal depending on the PCBs spacing as well as the number of the PCBs. The correlation derived in the previous section can be used to optimize the PCBs spacing. From the correlation (3) und (4) the Nusselt number can be expressed as:

$$Nu_p = ARa^B = \frac{\dot{Q}_p b}{2Sk\Delta T} \tag{5}$$

where A and B are constants, $\dot{Q}_p$ is heat dissipation on one PCB, b is PCBs spacing, S is one side area of the PCB. Under the same temperature difference the $\dot{Q}_p$ is a function of the PCBs spacing, which can be derived based on above equation:

$$\dot{Q}_p = Cb^{\frac{5B-1}{1-B}} \tag{6}$$

where C is constant. The total heat dissipation can be calculated as following:

$$\dot{Q} = N \cdot \dot{Q}_p = C\frac{l-b}{d+b}b^{\frac{5B-1}{1-B}} \tag{7}$$

where N is the number of the PCBs, which equals (l-b)/(d+b), d is the thickness of the PCB, l is the length of the casing. Differentiating equation (7) with respect to b, setting the derivative to zero leads to:

$$f(b) = D(l-b) - b\frac{d+l}{d+b} = 0 \tag{8}$$

Solving above equation yields the optimum PCBs spacing in the form:

$$E = d + l + D(d-l) \tag{9}$$

$$b_{opt} = \frac{\sqrt{E^2 + 4D^2dl} - E}{2D} \tag{10}$$

When the values of d=10.0 mm, l=170.0 mm and B=0.287 for the experiments are substitued in the above relation the optimum PCBs spacing is found to be 11.59 mm.

4 CONCLUSIONS

The results show that the unstable thermal boundary layer on the top wall of the casing plays an important role in natural convective air cooling of the PCBs array in a closed casing. Because of the thermal instability vortex flow and the temperature oscillation exist in the casing. Time-varying recirculation presents in the PCBs array. The heat transfer in such PCBs array is greatly influenced by the distance among the PCBs and relatively insensitive to the distance between the PCBs array and top wall or bottom wall. The average heat transfer coefficient on the top wall is 3 ~ 5 times higher than that on the bottom wall of the casing. The empirical correlations deduced from the experimental results and optimum PCBs spacing were presented in the paper.

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