Einladung zum Vortrag

Performance Engineering – Welcome to the World of FLOPs, Bytes and Cycles!

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We consider Performance Engineering (PE) as a structured, iterative process for code optimization and parallelization. The key ingredient is a performance model which provides insights into the interaction between the code and the hardware. The model identifies the actual performance-limiting factors ("bottlenecks"), allowing for a selection of appropriate code changes. Once the impact of the code changes is validated the process restarts with a new bottleneck identified by the performance model. This model-based approach provides a thorough understanding of the impact of hardware features on code performance and is useful in various other areas such as performance reproducibility, performance prediction for future architectures or education and training.

In the talk we first introduce our PE concept and survey basic "white-box" performance models [1,2] appropriate for performance modelling at the core- and node-level. Choosing a widely used benchmark suite [3] we demonstrate, that automatic "black-box" performance modelling may lead to misleading results if not used with due care. Focusing on selected kernels linear algebra and well as stencil computations [2] we show various aspects and application scenarios of our "white box" approach.

References

- [1] Williams, S., Waterman, A., and Patterson, D., Commun. ACM 52 (4), 65 (2009).
- [2] Stengel, H., Treibig, J., Hager, G., and Wellein, G., Proceedings of the 29th ACM on International Conference
- on Supercomputing (ICS 2015), 207 (2015).
- [3] McVoy, L. and Staelin, C., Proceedings of the 1996 annual conference on USENIX Annual Technical Conference (ATEC '96). USENIX Association, Berkeley, CA, USA, 23-23.

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